still protecting the underlying structure. The present invention therefore provides desirable misalignment tolerance which results in higher yields of processed semiconductor devices.

This invention defines a processing method for submicron geometries, and is most useful at geometries of less than 0.4 micron. The combined thin oxide and thick nitride layers afford a structure suitable for highly selective etching to define contact openings on the scale of 0.3 to 0.4 micron. The uniformly elevated and significantly wide landing plugs provide an easy target for conventional photolithographic techniques when forming the second contact openings. Additionally, the wide landing plugs provide misalignment tolerance which helps increase production yield.

In compliance with the statute, the invention has been described in language more or less specific as to methodical features. It is to be understood, however, that the invention is not limited to the specific features described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

We claim:

1. A semiconductor processing method of making electrical contact with an active area on a semiconductor wafer, the method comprising the following steps:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having sides;

providing an insulative layer on the sides of the conductive runners, the insulative sides of adjacent conductive runners being spaced a selected distance apart at a selected location on the wafer;

providing an active area between the conductive runners at the selected location;

providing a layer of first oxide to a selected thickness over the active area and conductive runners, the first oxide layer selected thickness being less than one-half the selected distance between the insulative sides of adjacent conductive runners;

providing a first planarized layer of insulating material atop the first oxide layer, the first layer of insulating material being selectively etchable relative to the first oxide, the first layer of insulating material having an upper surface;

patterning the planarized first insulating layer for definition of a first contact opening therethrough to the active area;

etching the patterned first insulating layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the planarized first insulating layer upper surface, the aperture width being greater than the selected distance between the insulative sides of adjacent conductive runners;

etching the first oxide layer within the first contact opening to expose the active area;

providing a plug of conductive material within the first contact opening over the exposed active area;

providing a second insulating layer over the first insulating layer and the conductive plug;

patterning and etching the second insulating layer to form a second contact opening to and exposing the conductive plug; and

providing a conductive layer over the second insulating layer and into the second contact opening, the conductive layer electrically contacting the conductive plug.

2. A semiconductor processing method according to claim 1 wherein the selected first oxide layer thickness is from about 100 to 1,000 Angstroms.

3. A semiconductor processing method according to claim 1 wherein the selected first oxide layer thickness is from about 300 to 500 Angstroms.

4. A semiconductor processing method according to claim 1 wherein the first insulating layer is formed of a nitride.

5. A semiconductor processing method according to claim 1 wherein the conductive plug is formed of polysilicon.

6. A semiconductor processing method according to claim 1 wherein the step of providing a first planarized layer of insulating material comprises:

providing a conformal first layer of insulating material atop the first oxide layer; and

chemical mechanical polishing the wafer to planarize the first insulating layer.

7. A semiconductor processing method according to claim 1 wherein the first insulating layer has an upper surface and wherein the step of providing a plug of conductive material comprises:

providing a layer of conductive material over the first insulating layer and within the first contact opening over the exposed active area;

chemical mechanical polishing the wafer to remove the conductive layer from the first insulating layer upper surface and to define a plug within the first contact opening, the plug having an upper surface slightly below the first insulating layer upper surface to ensure that the plug is electrically isolated.

8. A semiconductor processing method according to claim 1 wherein the second insulating layer is etched with an etchant selective to both the first insulating layer and the conductive plug.

9. A semiconductor processing method according to claim 1 wherein:

the first insulating layer is formed of a nitride;

the conductive plug is formed of polysilicon; and

the second insulating layer is etched with an etchant selective to both the nitride insulating layer and the polysilicon plug.

10. A semiconductor processing method for making electrical contact with an active area on a semiconductor wafer comprising the steps of:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having a top and sides;

providing insulative spacers on the sides of the runners, the insulative spacers being spaced a selected distance apart at a selected location on the wafer;

providing an active area between the conductive runners at the selected location;

depositing a first oxide layer over the wafer to a thickness from about 100 to 1,000 Angstroms, the first oxide layer having an upper surface defining a highest elevational location above the active area;

providing a nitride layer having an upper surface over the first oxide layer to a selected thickness, the nitride layer upper surface defining a lowest elevational location above the active area which is elevationally higher than the highest elevational location of the first oxide layer, the nitride being selectively etchable relative to the first oxide;

planarizing the nitride layer to a first elevational height above the active area, the first elevational height being higher than the highest elevational location of the first oxide layer;

patterning the planarized nitride layer for definition of a first contact opening therethrough to the active area;

etching the patterned nitride layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the nitride layer upper surface which is greater than the selected distance between the insulative sides of adjacent conductive runners;

etching the first oxide layer within the first contact opening to expose the active area;

providing a polysilicon plug within the first contact opening over the exposed active area to a second elevational height;

depositing a second oxide layer over the nitride layer and the polysilicon plug;

patterning and etching the second oxide layer to form a second contact opening to and exposing the polysilicon plug; and

providing a conductive layer over the second oxide layer and into the second contact opening, the conductive layer electrically contacting the conductive plug.

11. A semiconductor processing method according to claim 10 wherein the selected first oxide layer thickness is from about 300 to 500 Angstroms.

12. A semiconductor processing method according to claim 10 wherein the step of planarizing the nitride layer comprises chemical mechanical polishing the wafer to planarize the nitride layer.

13. A semiconductor processing method according to claim 10 wherein the step of providing a polysilicon plug comprises:

providing a layer of polysilicon over the nitride layer and within the first contact opening over the exposed active area;

chemical mechanical polishing the wafer to remove the polysilicon layer from the nitride layer upper surface and to define a polysilicon plug within the first contact opening.

14. A semiconductor processing method according to claim 10 wherein the second oxide layer is etched by an etchant selective to both the nitride layer and the polysilicon plug.

15. A semiconductor processing method according to claim 10 wherein the second elevational height is approximately equal to the first elevational height.

16. A semiconductor processing method according to claim 10 wherein the second elevational height is slightly lower than the first levational height.

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/17. A semiconductor processing method of forming an electrical contact structure for an active area on a semiconductor wafer, the method comprising the following steps:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having sides;

providing an insulative layer on the mutually adjacent sides of the conductive runners, the insulated mutually adjacent sides of adjacent conductive runners being spaced a selected distance apart;

providing an active area between the insulated mutually adjacent sides of conductive runners;

providing a layer of first oxide to a selected thickness over the active area and conductive runners, the first oxide layer selected thickness being less than one-half the selected distance between the insulated sides of adjacent conductive runners;

providing a first insulating layer having a planarized upper surface atop the first oxide layer, the first layer of insulating material being selectively etchable relative to the first oxide;

patterning the first insulating layer for definition of a first contact opening therethrough to the active area;

etching the patterned first insulating layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the first insulating layer planarized upper surface, the aperture width being greater than the selected distance between the insulated sides of adjacent conductive runners:

etching the first oxide layer within the first contact opening to expose the active area; and

providing a conductive plug of within the first contact opening over the exposed active area.

18. A semiconductor processing method according to claim 17 wherein the step of providing a plug of conductive material comprises:

providing a layer of conductive material over the first insulating layer and within the first contact opening over the exposed active area; and

polishing the wafer to remove the conductive layer from the first insulating layer planarized upper surface and to define the conductive plug within the first contact opening, the plug having an upper surface slightly below the first insulating layer planarized upper surface.

19. A semiconductor processing method according to claim 17 further comprising:

providing a second insulating layer and the conductive plug; and

patterning and etching the second insulating layer to form a second contact opening to expose the conductive plug.

20. A semiconductor processing method according to claim 19 further comprising etching the second insulating layer with an etchant selective to both the first insulating layer and the conductive plug.

21. A semiconductor processing method according to claim 19 further comprising:

forming the first insulating layer of a nitride;

forming the conductive plug of polysilicon; and

etching the second insulating layer with an etchant selective to both the nitride insulating layer and the polysilicon plug.

22. A semiconductor processing method of forming an electrical contact structure for an active area on a semiconductor wafer, the method comprising the following steps:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having sides;

providing an insulative layer on the mutually adjacent sides of the conductive runners, the insulated mutually adjacent sides of adjacent conductive runners being spaced a selected distance apart;

providing an active area between the insulated mutually adjacent sides of conductive runners;

providing a layer of first oxide to a selected thickness over the active area and conductive runners, the first oxide layer selected thickness being less than one-half the selected distance between the insulated sides of adjacent conductive runners;

providing a first insulating layer having a planarized upper surface atop the first oxide layer, the first insulating layer being selectively etchable relative to the first oxide, said step performed by,

providing a conformal first layer of insulating material atop the first oxide layers; and

polishing the wafer to planarize the first insulating layer upper surface;

patterning the first insulating layer for definition of a first contact opening therethrough to the active area;

etching the patterned first insulating layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the first insulating layer planarized upper surface, the aperture width being greater than the selected distance between the insulated sides of adjacent conductive runners;

etching the first oxide layer within the first contact opening to expose the active area; and

providing a conductive plug within the first contact opening over the exposed active area.

23. A semiconductor processing method for making electrical contact with an active area on a semiconductor wafer comprising the steps of:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having a top and sides;

providing insulative spacers on mutually adjacent sides of the runners, the insulative spacers being spaced a selected distance apart at a selected location on the wafer;

providing an active area between the conductive runners at the selected location;

depositing a first oxide layer over the wafer to a thickness from about 100 to 1,000 Angstroms, the first oxide layer having an upper surface defining a highest elevational location above the active area;

providing a nitride layer having an upper surface over the first oxide layer to a selected thickness, the nitride layer upper surface defining a lowest elevational location above the active area which is elevationally higher than the highest elevational location of the first oxide layer, the nitride being selectively etchable relative to the first oxide;

planarizing an upper surface of the nitride layer to a first elevational height above the active area, the first elevational height being higher than the highest elevational location of the first oxide layer upper surface;

patterning the nitride layer for definition of a first contact opening therethrough to the active area;

etching the patterned nitride layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the nitride layer upper surface which is greater than the selected distance between the insulative spacers at the mutually adjacent sides of the conductive runners;

etching the first oxide layer within the first contact opening to expose the active area;

providing a polysilicon plug within the first contact opening over the exposed active area to a second elevational height; and

depositing a second oxide layer over the nitride layer and the polysilicon plug.

24. A semiconductor processing method according to claim 23 wherein the step of planarizing the nitride layer comprises polishing the wafer to planarize the nitride layer.

25. A semiconductor processing method according to claim 23 wherein the step of providing a polysilicon plug comprises:

providing a layer of polysilicon over the nitride layer and within the first contact opening over the exposed active area; and

polishing the wafer to remove the polysilicon layer from the nitride layer upper surface and to define a polysilicon plug within the first contact opening.

26. A semiconductor processing method according to claim 23 further comprising etching the second oxide layer by an etchant selective to both the nitride layer and the polysilicon plug.

N:\2269\3255.1\New claims